Notice of Allowability	Application No. 09/275,495	Applicant(s) GARTSTEIN ET AL.	
	Examiner Julian Mercado	Art Unit 1745	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9-29-03 and 2-2-04*.

2. ☒ The allowed claim(s) is/are *1-12, 14-22 and 24-29*.

3. ☒ The drawings filed on *24 March 1999* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Remarks

This Office action is responsive to applicant's amendment filed September 29, 2003 and February 2, 2004.

Claim Rejections - 35 USC § 103

The rejection of claims 1-7 and 24-27 under 35 U.S.C. 103(a) based on Nagai et al. has been withdrawn.

The rejection of claims 8-11 under 35 U.S.C. 103(a) based on Nagai et al. and Stewart has been withdrawn.

In withdrawing the prior art rejections above based primarily on Nagai et al. the examiner would like to make the following remarks on record. Applicant on page 15 of the present response states:

> Rather than responding to the substance of this assertion, the Examiner in the Office Action of 10/2/01 (page 2) makes the bald statement that "As discussed in a prior Office Action, the circuit is also responsive to the cell internal impedance exceeding a predetermined impedance, wherein such a condition prompts uncoupling of the voltage and preventing discharge". However, there is no "prior Office Action" that discusses this concept.

Applicant's attention is directed to the Office action dated October 2, 2000, wherein the paraphrased portion of the examiner's reasoning above may be found, verbatim, under a then-102(e) discussion of Nagai et al. in col. 9 line 40 et seq. and col. 16 line 59 et seq.

Applicant further states the following:

> Further, the Examiner makes not (sp) attempt to explain how, whatever circuit he is referring to, could possibly measure internal impedance through the use of an external resistance R0.

The examiner is at a loss as to why applicant is of the belief that the prior Office action relied on the external resistor R0 to read on applicant's variable impedance feature. Since none of the prior Office actions nor the present one relies on the external resistor R0 in this manner, the examiner herein makes no attempt to rectify applicant's assertion that such a position allegedly taken by the examiner is improper.

It is the examiner's position that applicant inferred, incorrectly, that the prior Office action relied on the resistor R0 as an internal impedance feature of the battery based on the examiner's citation of col. 9 line 40-56 of Nagai et al., wherein it states:

> When the control circuit 12 monitors the change of the output voltage in step 219, an impedance of the transistor FET2, for example, may be changed to detect the change of the voltage across both ends of the resistor R0 at that time. Specifically, as shown in FIG. 6, if a residual capacity of the secondary battery 11 is within a normal range, then a voltage V_1 across both ends of the resistor R0 is gradually increased when the impedance Z_1 of the transistor FET2 is gradually lowered after the beginning of the discharge. If the increase of the voltage V_1 is detected, then it may be determined that the secondary battery 11 is in its dischargeable state, thereby the discharge operation being continued. If on the other hand the voltage V_1 across both ends of the resistor R0 is not increased even when the impedance Z_1 is gradually lowered, then it is determined that the residual capacity of the secondary battery 11 is small, and the discharge operation is stopped.

A careful reading of the above cited section of Nagai et al.'s disclosure will reveal that the basis for the examiner's reasoning that, indeed, the battery of Nagai et al. is responsive to a predetermined condition substantially determined by an internal impedance level is dependent upon the disclosed transistor FET2 which in itself has a detectable and variable impedance level.

Allowable Subject Matter

Claims 1-12, 14-22 and 24-29 are allowed.

Claims 12, 14-22, 28 and 29 are allowed for the reasons set forth in the previous Office action.

Claims 1-11 and 24-27 are allowed for the following reasons: The examiner's remarks above have been made on record to negate applicant's assertions of any misunderstandings by the examiner in consideration of the claims prior to the present amendment, e.g. applicant states on page 15 of the present response that "[t]he response of 3/17/03 attempted to help the Examiner understand the basis of his misunderstanding" etc. In making these remarks it is hoped that the reasons for allowance of claims 1-11 and 24-27 may be understood as being based not on withdrawal of the prior art rejections as applied to the claims prior to the present amendment, but more so in view of the present amendment further defining the claimed invention. The examiner notes that the present amendment further defines independent claims 1 and 24 to recite that the predetermined condition is/are "substantially determined by said internal impedance reaching a predetermined impedance level". (the present amendment to the claims indicated in the underlined portion) It can be appreciated from col. 9 line 40-56 of Nagai et al. (as quoted above) that the internal impedance of transistor FET2 is varied in order to detect "the change of the *voltage* across both ends of the resistor R0 at that time". [emphasis added] That is, in Nagai et al. it is the voltage (and not the internal impedance) that is detected to reach a predetermined level, during which the internal impedance itself is varied to detect the effects of such a change in the measured voltage. Applicant's claimed invention is detecting a change in the internal impedance reaching a predetermined impedance level, while Nagai et al. detects a change (increase or decrease) in the voltage reaching a predetermined impedance level during the lowering of the impedance of transistor FET2.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. UK Patent Application GB 2 271 288 A is cited to teach a battery in which a predetermined impedance level results in "imminent battery exchange" and "shutting down of the connected system" (page 4), however, the controller [9] does not form an output or cell voltage across positive and negative electrodes of the battery cell as required by the present invention. This feature of the instant controller forming an output voltage of the battery cell is understood by the examiner as best illustrated in Figure 4 of applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julian Mercado whose telephone number is (571) 272-1289. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Ryan, can be reached on (571) 272-1292. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

jam

Patrick Ryan
Supervisory Patent Examiner
Technology Center 1700